NETLOGIC MICROSYSTEMS INC
Form 10-K
March 11, 2005
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UNITED STATES

SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

FORM 10-K

(Mark One)

x ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934

For the fiscal year ended December 31, 2004

or

¨ TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934

For the transition period from _____ to _____

COMMISSION FILE NO.: 000-50838

NETLOGIC MICROSYSTEMS, INC.

(Exact name of Registrant as specified in its charter)

DELAWARE	**77-0455244**
(State or other jurisdiction of incorporation or organization)	**(I.R.S. Employer Identification No.)**

1875 Charleston Road

Mountain View, California 94043

(650) 961-6676

(Address, including zip code, and telephone number, including area code, of the registrant s principal executive offices)

SECURITIES REGISTERED PURSUANT TO SECTION 12(b) OF THE ACT:

None

SECURITIES REGISTERED PURSUANT TO SECTION 12(g) OF THE ACT:

COMMON STOCK, par value $.01 per share

Indicate by check mark whether the registrant: (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes x No ¨

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of the registrant s knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K. x

Indicate by check mark whether the registrant is an accelerated filer (as defined in Rule 12b-2 of the Exchange Act). Yes ¨ No x

The aggregate market value of the registrant s common stock held by non-affiliates of the registrant, based upon the closing sale price of the Common Stock on February 28, 2005 as reported on the Nasdaq National Market, was $123,857,841. This calculation does not reflect a determination that certain persons are affiliates of the Registrant for any other purpose.

As of February 28, 2005, registrant had outstanding 17,679,857 shares of common stock, its only class of voting or non-voting common equity.

DOCUMENTS INCORPORATED BY REFERENCE

Portions of the Registrant s proxy statement to be delivered to the stockholders in connection with registrant s 2005 Annual Meeting of Stockholders to be held on or about May 18, 2005, are incorporated by reference into Part III of this Form 10-K. The registrant intends to file its proxy statement within 120 days after its fiscal year end.

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FISCAL 2004 FORM 10-K

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PART I

Forward-looking Statements

This report contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933, as amended, and Section 21E of the Securities Exchange Act of 1934, as amended, which include, without limitation, statements about the market for our technology, our strategy and competition. Such statements are based upon current expectations that involve risks and uncertainties. Any statements contained herein that are not statements of historical fact may be deemed forward-looking statements. For example, the words believes , anticipates , plans , expects , intends and similar expressions are intended to identify forward-looking statements. Our actual results and the timing of certain events may differ significantly from the results discussed in the forward-looking statements. Factors that might cause such a discrepancy include, but are not limited to, those discussed in Overview , Results of Operations, Liquidity and Capital Resources and Risks Factors below. All forward-looking statements in this report are based on information available to us as of the date hereof and we assume no obligation to update any such forward-looking statements. The information contained in this report should be read in conjunction with our condensed financial statements and the accompanying notes contained herein. Unless expressly stated or the context otherwise requires, the terms we , our , us and NetLogic Microsystems refer to NetLogic Microsystems, Inc.

ITEM 1. BUSINESS.

Overview

We are a semiconductor company that designs, develops and markets high performance knowledge-based processors for a variety of advanced Internet, corporate and other networking systems, such as routers, switches, network access equipment and networked storage devices. Knowledge-based processors are integrated circuits that employ an advanced processor architecture and a large knowledge database containing network and network user information to make complex decisions about individual packets of information travelling through the network. Our knowledge-based processors significantly enhance the ability of networking original equipment manufacturers, or OEMs, to supply network service providers with systems offering more advanced functionality for the Internet, such as voice transmission over the Internet, or VoIP, virtual private networks, or VPNs, and streaming video and audio.

Prior to our development of knowledge-based processors, we developed integrated circuits to address basic forwarding functions used in networking systems for the core and enterprise networking markets. We introduced our first product in July 1997, which was sold in limited quantities. To respond to evolving networking requirements, we developed our next generation of products, our network search engines, which featured more advanced processing capabilities. From 1998 to 2001, we introduced several of these network search engine products. During this time, our revenue from these products was low, and we experienced significant net operating losses. In 2000, in response to the dramatic growth in and greater complexity of Internet traffic, we recognized the need to develop more advanced processors to enable higher performance for a variety of advanced networking systems. By 2001, we were able to broaden our customer base to include networking OEMs such as Cisco Systems, Inc., Huawei Technologies Co., Ltd. and Nortel Networks Corporation. In 2002, we introduced our knowledge-based processors, and began substantial production in the second half of 2003, resulting in the majority of our revenue in 2003 and 2004.

Our knowledge-based processors incorporate advanced technologies that enable rapid processing, such as a superscalar architecture, which uses parallel-processing techniques, and deep pipelining, which segments processing tasks into smaller sub-tasks, for higher decision throughput. These technologies enable networking systems to perform a broad range of network-aware processing functions, such as access control for network security, prioritization of traffic flow to maintain quality of service, or QoS, and statistical measurement of Internet traffic for

transaction billing.

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We design our products at the transistor level and use a full-custom layout flow to define how circuits are constructed in silicon. This allows us to optimize circuit design, minimize chip size and reduce power dissipation of our integrated circuits. By minimizing chip size, we are able to optimize the cost of our knowledge-based processors and facilitate the design of our customers products within smaller enclosures, or form factors.

We provide complete, systems-level solutions that include interface designs and firmware, device driver, packet-processing and knowledge database management application software, design tools and environments and reference designs. By providing a comprehensive systems-level solution, we help networking OEMs reliably introduce next generation networking systems and significantly enhance their time-to-market. These systems-level solutions are provided free-of-charge to our OEM customers to encourage sales of our products.

Our products are designed into systems offered by leading networking OEMs, including Alcatel, ARRIS Group, Inc., Atrica, Inc., Cisco, CloudShield Technologies, Inc., Extreme Networks, Inc., Fujitsu Limited, Hitachi, Ltd., Huawei, Juniper Networks, Inc. and Nortel Networks. We organized our business in 1995 as a California limited liability company and, incorporated in Delaware in 2000.

Industry Overview

Networking Market Overview

The Internet has experienced dramatic growth and evolved significantly due to a sharp increase in the level of worldwide voice, video and data traffic. According to International Data Corporation (IDC, 2003), total worldwide Internet traffic is expected to increase from 180 petabits per day in 2002 to 5,175 petabits per day in 2007. This represents a compound annual growth rate of 95.7%. This growth has been driven primarily by a wider variety of uses for the Internet, an increased amount of digital media content available through the Internet, and more advanced Internet applications. These applications include:

Voice transmission over the Internet, or VoIP;

Video on demand, or VoD;

Streaming video and audio;

Music, picture and video file downloading and sharing;

Email communications; and

E-commerce.

Due to the rapid growth of voice, video and data traffic, as well as the greater complexity created by the convergence of these types of traffic, there has been significant expansion of the global networking infrastructure using advanced packet-switching protocols, which are the data formats that enable communication among the systems within the network. These networking systems, based upon packet-switching protocols, transport packets of information through the network. The most common packet-switching protocol is the Internet Protocol, or IP.

The Internet infrastructure consists of various networking systems that handle the processing of IP packets. These systems include routers, switches, network access equipment and networked storage devices. An IP packet that is sent from one user s device to another typically travels through a variety of networks that comprise the Internet infrastructure. These types of networks include:

core networks, for long-distance city-to-city communications which may span hundreds or thousands of miles;

enterprise networks, for internal corporate communications, including access to storage environments;

metro networks, for intra-city communications which may span several miles;

edge networks, which link core, metro, enterprise and access networks; and

access networks, which connect individual users to the edge network.

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The following diagram depicts typical network connections within the Internet infrastructure:

IP packets are transferred from one networking system to another through these network connections. Each system within the network and each connected end-user device, such as a computer, is assigned a unique identifier, known as an IP address, which allows these systems and devices to communicate with each other. Decisions on how to handle IP packets are made using the data that is contained in the packet header. The packet header information consists of key data regarding the packet, including the IP address of the system that generated the packet, referred to as the source IP address, and the IP address of the device to which the packet is to be transmitted, referred to as the destination IP address. When a packet arrives at a networking system such as a switch or a router, the packet is processed and decisions about the packet header are made. For example, an IP packet traveling from New York to San Francisco might travel through as many as 15 routers or switches and be processed a number of times by each router or switch. For many networking applications, packet processing must be performed without slowing down the overall flow of communication. Keeping pace with the rate of communication flow is referred to as wire-speed performance.

Transporting a packet from its source to a destination involves a basic class of packet processing commonly known as forwarding. For example, to forward a packet, a switch or router would use a packet processor to extract the header information from an incoming packet and store the information to be transported temporarily in an area known as the buffer. Next, the packet header information, in particular

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the destination IP address, would be analyzed to establish the networking system that the packet should be forwarded to in order to move the packet one step closer to its final destination. Networking OEMs implement packet processor functionality either by developing their own custom integrated circuit solutions, or by using network processors, or NPUs, developed by third parties.

Due to the increased usage of the Internet, as well as the greater complexity of Internet-based applications, the amount of processing required for packets is increasing significantly. These more complex applications require multiple classes of packet processing that depend on both the type of content being transported and the information, or knowledge, of the overall network.

Trend Towards Network-aware Processing

Rapid growth of voice, video and data traffic, as well as the greater complexity created by the convergence of these types of traffic, increasingly challenges OEMs to offer systems that enable network service providers to introduce new services over the Internet, such as VoIP, VPNs, video on demand, streaming video and audio and music file downloading. In particular, networking OEM systems must increasingly use knowledge about the overall network, which includes the method and manner in which networking systems are interconnected as well as traffic patterns and congestion points, connection availability, user-based privileges, priorities and other attributes. Using this knowledge to make complex decisions about individual packets of information involves network awareness, which includes the following:

- Preferential transmission of packets based upon assigned priority;
- Restrictions on access based upon security designations;
- Changes to packet forwarding destinations based upon traffic patterns and bandwidth availability; and
- Addition or deletion of information about networks and users.

Network awareness in advanced systems requires multiple classes of packet processing, in addition to forwarding. These additional classes of processing include access control for network security, prioritization of packets to maintain QoS and statistical measurement of Internet traffic for transaction billing. Compared to the basic processing task of forwarding, these additional classes of packet processing require a significantly higher degree of processing of IP packets to enable network awareness, or network-aware processing. To maintain wire-speed performance in a network-aware environment, major networking OEMs require hundreds of millions of packet decisions each second, while also updating the knowledge database up to 100,000 times per second.

Several powerful trends are driving greater demand for network-aware processing:

- *Increasing Internet traffic drives the need for higher bandwidth*. New applications continue to emerge, including applications for file sharing and downloading of digital media such as MP3 audio files and digital images such as photographs. These new applications require greater speed for effective transmission, which is driving the need for higher bandwidth. To satisfy these needs, routers, switches and other networking systems must have the ability to make rapid forwarding decisions that determine what further processing should be done for the packet, identify where the packet should be sent to next and rapidly transport the packet to the

destination port. For example, edge and metro networking speeds have evolved from 1 Gigabit per second, or 1 Gb/s, to 2.5 Gb/s, and are expected to increase to 10 Gb/s over the next several years.

Increasing network security requires additional packet inspection. In order to make IP networks secure, security technologies are being deployed at various points within the global networking infrastructure. For example, in the enterprise network, features are being added to secure specific links using VPNs and access control lists. VPNs prevent eavesdropping on a secured communications link that is established between two devices and access control lists enable network service providers to permit or deny access to certain destinations. To implement these features, additional packet inspection is needed, which is

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typically more complex than the basic processing for forwarding decisions. These features require more information to be stored in the knowledge database and to be subsequently extracted for processing.

Convergence of voice, video and data traffic requires enhanced QoS. Convergence of voice, video and data traffic requires enhancement of the IP network infrastructure, as these new services have more stringent performance requirements than traditional packet data. For example, delay in the transmission of a packet, or latency, would significantly degrade the quality of voice and video communications. To support more advanced communications, the network needs to treat packets of data in the IP network differently by assigning them a specified QoS level. For example, packets that require time-critical delivery can be assigned a higher priority for transmission, thereby reducing latency.

Proliferation of Internet-connected devices requires more complex processing capabilities and larger knowledge databases. Each Internet-connected device, including computers, handheld personal digital assistants and data and video-enabled mobile phones, is assigned an IP address. The significant increase in the number of such devices has led to a corresponding increase in the number of devices that networking systems need to support, requiring larger knowledge databases. In addition, in an effort to accommodate the connection of more devices to the Internet, the networking industry is moving to a new protocol standard, Internet Protocol version 6, or IPv6, which will increase the length of each IP address, requiring significantly more complex network-aware processing to support larger knowledge databases.

The multiplicative effect of these trends leads to a significantly greater need for advanced processing that utilizes overall knowledge of the network to enable network awareness within switches, routers and other networking systems. Higher levels of performance are required to enable advanced processing for a greater variety of packet processing, such as access control for network security, prioritization of packets to maintain QoS and statistical measurement of Internet traffic for transaction billing, in addition to the forwarding functions.

Networking OEMs have used several approaches to enable network awareness in their systems. One approach involves the use of internally designed custom integrated circuit solutions. Other OEMs have chosen to outsource this requirement to merchant integrated circuit suppliers. Networking OEMs use these integrated circuits to analyze and make decisions about an IP packet based on the packet s header information, which is extracted by the OEMs packet processors. The packet processor inspects the specific implementations of packet-switching protocols and executes specific instructions needed to move the packet through the networking system.

The custom integrated circuit and merchant approaches have both been adequate for the basic decision-making required for forwarding, particularly at lower speeds. However, as the demand for bandwidth and the need to support more advanced Internet applications increases, these approaches are increasingly unable to scale at the pace demanded by advanced applications because of their slower and less efficient processing capability. This creates a bottleneck in the information flow and limits overall system performance. Further, in designing high performance systems, networking OEMs need to address other performance issues, such as power dissipation. Minimizing the power dissipated by integrated circuits is becoming more important for networking systems such as routers and switches, which are increasingly designed in smaller form factors.

Networking OEMs face growing pressure to rapidly introduce new products, reduce their design and manufacturing costs and respond to the growing demand from network service providers for new and advanced services. These OEMs choose to focus on their core competencies in the design and development of certain functionalities within their networking systems, as well as systems-level design and integration. As a result, networking OEMs increasingly seek third party providers of advanced processing solutions that complement their core competencies to enable network awareness within their systems and meet their escalating performance requirements for rapid processing speeds, complex decision-processing capabilities, low power dissipation, small form factor and rapid time-to-market.

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Our Solution

To enable network awareness for a variety of advanced networking systems, such as routers, switches, network access equipment and networked storage devices, we offer high performance knowledge-based processors. Our knowledge-based processors use an advanced processor architecture and a large knowledge database containing network and network user information to make complex decisions about individual packets of information travelling through the network. These features enable advanced processing across a variety of classes of packet processing, including access control for network security, prioritization of packets to maintain QoS and statistical measurement of Internet traffic for transaction billing. In addition, we design our products by connecting individual transistors and we use a full-custom layout flow to define precisely how circuits are constructed in silicon, enabling us to optimize circuit design, minimize chip size and reduce power dissipation of our integrated circuits.

Key features of our solution include:

Advanced Architecture for High-Speed Performance. Our knowledge-based processors enable networking OEMs to offer products that process packets at wire-speed performance. Our knowledge-based processors are designed with a superscalar architecture that enables multiple decisions to be processed in parallel. In addition, our knowledge-based processors employ deep pipelining, which segments processing tasks into smaller sub-tasks for higher decision throughput. We use these advanced technologies to enable faster decision throughput in the network. In addition, our knowledge-based processors include features that give access to and support multiple NPUs, allowing more than one NPU to handle packet processing simultaneously. By incorporating our products, networking OEMs are able to process packets more rapidly.

Expandable Processing Resources. We offer knowledge-based processors that can process packets using knowledge databases containing up to approximately 512,000 records on a single integrated circuit. Additionally, our customers can interconnect multiple knowledge-based processors, which extends the usable knowledge database to up to approximately four million records. This allows our OEM customers products to support a range of decision-making capacities that scales with end-user requirements. This feature becomes more critical as the number of devices connected to the Internet increases and networking OEMs deploy IPv6, creating the need for additional processing resources and larger knowledge databases to support longer IP addresses.

Full-Custom Integrated Circuit Design for Reduced Cost and Low Power Dissipation. We design our products using full-custom methodologies that allow us to optimize circuit area to implement specific functionality and accommodate larger knowledge databases. Our use of a full-custom layout flow allows for enhanced control of transistor characteristics as needed for optimized circuit design and enables us to minimize chip size and reduce power dissipation of our integrated circuits. By minimizing chip size, we are able to optimize the cost of our knowledge-based processors and facilitate the design of our OEM customers products within smaller form factors.

Systems-Level Solutions for Enhanced Design Flexibility and Rapid Time-to-Market. To encourage our customers to design into their products our knowledge-based processors and to assist their design efforts, we offer various systems-level solutions. These include designs for programmable products that interface a customer s custom integrated circuits with our knowledge-based processors, software and firmware to program our knowledge-based processors and products that interface with our knowledge-based processors, and design tools and environments and reference designs that facilitate the incorporation of our knowledge-based processors into a customer s system. We do not charge our customers for providing these system-level solutions. We work with NPU providers to validate our reference hardware and software, so that networking OEMs using our reference hardware and software can design their products with our knowledge-based processors more reliably and move to production more quickly. We also provide without charge dedicated applications support to enhance the product time-to-market for our OEM customers who choose to develop their own interfaces to our products.

Transistor-Level Circuit Design for Enhanced Performance. In order to meet the stringent demands of our knowledge-based processors for high speed, low power dissipation and small form factors, we use a highly

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customized design approach using transistor-level circuit designs. By using a highly customized design flow, we are able to control precisely how the processing elements are constructed in silicon, leading to higher levels of integrated circuit performance. Designing integrated circuits at the transistor level requires a deep understanding of device physics to maximize transistor device performance. We employ simulation tools that are commonly used in the transistor-level design of analog integrated circuits. We complement these tools with our proprietary techniques to meet the complex design requirements of our knowledge-based processors.

Our Strategy

Our objectives are to be the leading provider of network-aware processing solutions to networking OEMs and to expand into new markets and applications. To achieve these goals, we are pursuing the following strategies:

Maintain and Extend our Market and Technology Leadership Positions. We were the first supplier of knowledge-based processors with approximately 512,000 records, the first supplier to achieve 1.0 Volt operation of knowledge-based processors for lower power dissipation, and the first supplier to achieve operating frequencies of over 300 MHz. We intend to expand our market and technology leadership positions by continuing to invest in the development of successive generations of our knowledge-based processors to meet the increasingly high performance needs of networking OEMs. We intend to leverage our engineering capabilities and continue to invest significant resources in recruiting and developing additional expertise in the area of high performance circuit design, custom circuit layout, high performance I/O interfaces, and applications engineering. By utilizing our proprietary design methodologies, we intend to continue to target the most demanding, advanced applications for our knowledge-based processors.

Focus on Long-Term Relationships with Industry-Leading OEM Customers. The design and product life cycles of our OEM customers products have traditionally been lengthy, and we work with our OEM customers at the pre-design and design stages. As a result, our sales process typically requires us to maintain a long-term commitment and close working relationship with our existing and potential OEM customers. This process involves significant collaboration between our engineering team and the engineering and design teams of our OEM customers, and typically involves the concurrent development of our knowledge-based processors and the internally-designed packet processors of our OEM customers. We intend to continue to focus on building long-term relationships with industry-leading networking OEMs to facilitate the adoption of our products and to gain greater insight into the needs of our OEM customers.

Leverage Technologies to Create New Products and Pursue New Market Opportunities. We intend to leverage our core design expertise to develop our knowledge-based processors for a broader range of applications to further expand our market opportunities. We plan to address new market segments that are increasingly adopting network-aware processing, such as corporate storage networks, which increasingly use IP-based packet-switching networking protocols.

Capitalize on Highly Focused Business Model. We are a fabless semiconductor company, utilizing third parties to manufacture, assemble and test our products. This approach reduces our capital and operating requirements and enables us to focus greater resources on product development. We work closely with our wafer foundries to incorporate advanced process technologies in our solutions to achieve higher levels of performance and reduced cost. These technologies include advanced complementary metal oxide semiconductor, or CMOS, implemented in a 0.13 micron logic process flow, up to eight layers of copper interconnect and 300 millimeter wafer sizes. Our business model allows us to benefit from the large manufacturing investment of our wafer foundries who are able to leverage their investment across many markets.

Expand International Presence. We sell our products on a worldwide basis and utilize a network of direct sales and independent sales representatives in the U.S., Europe and Asia. We intend to continue to expand our sales and technical support organization to broaden our

customer reach in new markets. We believe that Asia, in

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particular China, where we have already established customer relationships, provides the potential for significant additional long-term growth for our products. Given the continued globalization of OEM supply chains, particularly with respect to design and manufacturing, we believe that having a global presence will become increasingly important to securing new customers and design wins and to support OEMs in bringing their products to markets.

Our Markets and Products

Our products are incorporated in a broad variety of networking systems that handle the processing of IP packets. These systems are used throughout multiple types of networks that comprise the global Internet infrastructure, including the enterprise, metro, access, edge and core networking markets. These networks vary in their requirements for bandwidth, number of users to support and complexity of IP packet processing. For example, the core networking market has very high bandwidth requirements, as it typically handles traffic from many individual users, to enable Internet traffic over distances that typically span hundreds or thousands of miles. Our OEM customers networking systems in the core network typically incorporate several of our knowledge-based processors to provide very large knowledge databases to accommodate large numbers of users. Due to the increased usage of the Internet, as well as the higher complexity of Internet-based applications, we expect network-aware processing to increasingly become a more essential component of networking systems throughout the global Internet infrastructure.

Key characteristics of our knowledge-based processors include:

- Superscalar architectures, which increase decision throughput by executing multiple decisions in parallel;
- Flexible allocation of network-aware processing resources among different classes of packet processing, which allows different subsets of the knowledge database to be selected;
- Deep pipelining, which segments processing tasks into smaller sub-tasks for higher decision throughput; and
- A comprehensive set of instructions to implement network-aware processing.

We offer a broad range of our knowledge-based processors in two main product families.

Proprietary Interface Knowledge-based Processors NL5000 Family

Our proprietary interface knowledge-based processors are used primarily by networking OEMs developing their own packet processors. Our products operate in conjunction with an OEM-developed custom integrated circuit or a programmable logic device, such as a field programmable gate array, and feature a proprietary interface that provides advanced interface technology to enable networking OEMs to meet their demanding system performance requirements.

Networking OEMs typically require solutions at different prices in order to target different market segments with the same design. To satisfy this demand, our proprietary interface knowledge-based processor family incorporates product offerings with a range of knowledge database sizes, and all of our knowledge-based processors are designed to be connected in groups to increase the knowledge database available for processing.

We introduced our proprietary interface knowledge-based processors, which are designed in a 0.13 micron TSMC logic process, to the market in the second quarter of 2002. These processors operate from a 1.0 Volt power supply for reduced power consumption and support a knowledge database of up to approximately 512,000 records with performance of up to 500 million decisions per second. These processors also support advanced features for improved fault tolerance that help maintain the data integrity of the knowledge database by providing built-in circuitry to detect faults in the knowledge database.

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We also provide versions of our proprietary interface knowledge-based processors that work with proprietary custom integrated circuits and application software developed by Cisco.

NPU Interface Knowledge-based Processors NL5000GLQ Family

Our NPU interface knowledge-based processors are designed to interface directly to NPUs, such as those from Intel Corporation. They incorporate architectural features that simultaneously support multiple NPUs and NPU-based designs, resulting in more rapid packet processing. These features enable a single knowledge-based processor to make network-aware decisions for both incoming and outgoing communications line channels.

We introduced our NPU interface knowledge-based processors, which are designed in a 0.13 micron TSMC logic process, to the market in the first quarter of 2004. These processors operate from a 1.0 Volt power supply for reduced power consumption and support a knowledge database of up to approximately 512,000 records with performance of up to 125 million decisions per second.

The following table summarizes our current knowledge-based processor offerings:

Product	Introduction Date	Process Technology	Performance	Key Features
NL5000 Family (including a customized version for Cisco)	Q2 2002	0.13 micron TSMC logic process	Up to 500 million decisions per second	High performance through a superscaler architecture and deep pipelining Knowledge database with advanced configurability supporting up to approximately 512,000 records Support for fault tolerance in the knowledge database Operate from 1.0 Volt power supply for low power consumption Support for Cisco custom instruction set (available with Cisco version only)
NL5000GLQ Family	Q1 2004	0.13 micron TSMC logic process	Up to 125 million decisions per second	High performance through a superscaler architecture and deep pipelining

Knowledge database with advanced configurability supporting up to approximately 512,000 records

Direct interface to and simultaneous support for two network processors

Operate from 1.0 Volt power supply for low power consumption

Knowledge-based Processors Under Development

We are actively developing proprietary interface and NPU interface knowledge-based processors using CMOS logic manufacturing processes with geometries of 0.90 microns and higher with up to eight layers of copper interconnect. These new designs will enable us to offer knowledge-based processors that feature higher levels of performance, including additional functionality developed in close cooperation with our customers to improve application-specific performance.

NETLite Processors

Our NETLite NL3100 processor product family is specifically designed for cost-sensitive, high-volume applications such as entry-level switches, routers and access equipment. The NETLite processor family leverages

NPU Interface

Knowledge-based Processors

Proprietary Interface
Knowledge-based Processors

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circuit techniques developed and refined during the design of our knowledge-based processor families, and benefits from die size optimization, lower power dissipation and redundant computing techniques. In addition, the NETLite processor s simplified pipeline architecture allows for lower cost manufacturing and assembly in less expensive packages than our knowledge-based processors, and allows for lower cost system designs. As such, the NETLite processors are ideal for entry-level systems that do not require the advanced parallel processing and deep pipelining performance of our high-end knowledge-based processors.

For rapid time to market, our customers can use our software development kit, or NLSDK, to develop and verify hardware and software using the NETLite processors. The NLSDK allows customers to run cycle-accurate patterns at varying operating speeds to exercise the functionality of the NETLite processors and confirm compatibility with target applications. The NETLite processor family is also supported by a suite of production qualified firmware and software drivers and system reference designs, which will enable the growing entry-level system segment to more quickly ramp production with new designs supporting next-generation Internet features such as QoS, security and Layer 3 routing.

The following table summarizes our current NETLite processor offerings:

Product	Introduction Date	Process Technology	Performance	Key Features
NL3100 Family	Q1 2005	0.13 micron TSMC logic process	Up to 80 million decisions per second	Simplified pipelined architecture Simplified instruction set, which is a subset of the knowledge-based processor instruction set Lower cost manufacturing and system designs NLSDK development kit Hardware and software reference platforms

Legacy Products

We continue to support our legacy network search engines, which include the NL1000 through NL4000 network search engine families and the NL3128GLM network search engines, a device that interfaces directly to certain NPUs from Applied Micro Circuits Corporation. We introduced our network search engine products between 1998 and 2001. These products are fabricated by UMC or TSMC using a range of process technologies from 0.35 micron to 0.15 micron.

We also continue to support a legacy classification and forwarding processor, or CFP, product, that provides certain advantages over NSEs for particular classes of packet processing commonly used in networking systems. We introduced the CFP, which is fabricated by UMC using a 0.25 micron process, to the market in the second quarter of 2000. We continue to research CFP technology and may incorporate it into a future knowledge-based processor product.

Customers

The markets for networking systems utilizing our products and services are mainly served by large networking OEMs, such as Alcatel, ARRIS, Atrica, Cisco, Cloudshield, Extreme Networks, Force 10 Networks, Foundry Networks, Inc., Fujitsu, Hitachi, Huawei, Juniper Networks and Nortel Networks. We work with these and other networking OEMs to understand their requirements, and provide them with solutions that they

then qualify and, in some cases, specify for use within their systems. While we sell directly to some networking OEMs, we also provide our products and services indirectly to other networking OEMs through their contract manufacturers, who in turn assemble our products into systems for delivery to our OEM customers. Sales to contract manufacturers accounted for 78%, 38% and 27% of total revenue in 2004, 2003 and 2002, respectively. Sales of our products are made under short-term, cancelable purchase orders. As a result, our ability to predict future sales in any given period is limited and subject to change based on demand for our OEM customers systems and their supply chain decisions.

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We also provide our products and services indirectly to our OEM customers through our international stocking sales representatives. Our stocking sales representatives are independent entities that assist us in identifying and servicing foreign networking OEMs and generally purchase our products directly from us for resale to OEMs or contract manufacturers located outside the U.S. Our international stocking sales representatives generally exclusively service a particular foreign region or customer base, and purchase our products pursuant to cancellable and reschedulable purchase orders containing our standard warranty provisions for defects in materials, workmanship and product performance. At our option, defective products may be returned for their purchase price or for replacement. To date, our international stocking sales representatives have returned a small number of defective products to us. Our international stocking sales representatives may also act as a sales representative and receive commissions on sales of our products. Our international stocking sales representatives include Bussan Microelectronics Corporation/Mitsui Comtek Corporation and Lestina International Limited. Sales through our international stocking sales representatives accounted for 12%, 22% and 19% of total revenue in 2004, 2003 and 2002, respectively. While we have purchase agreements with our international stocking sales representatives, our international stocking sales representatives do not have long-term contracts with any of our OEM customers that use our products and services.

In 2004, Cisco, including its contract manufacturers, accounted for 73% of our total revenue. In 2003, Solectron (as Cisco s contract manufacturer), Micron Technology, Inc. and Bussan Microelectronics /Mitsui Comtek accounted for 27.4%, 25.9% and 15.5% of our total revenue, respectively. In addition, in 2003, Cisco, including its contract manufacturers, accounted for 33.5% of our total revenue. In 2002, Cisco, including its contract manufacturers, accounted for 21.6% of our total revenue.

Sales and Marketing

Our sales and marketing strategy is to achieve design wins with leaders and emerging participants in the networking systems market and to maintain these design wins primarily through leading-edge products and superior customer service. We focus our marketing and sales efforts at a high organizational level of our potential customers to access key decision makers. In addition, as many networking OEMs design custom integrated circuits to interface to our products, we believe that applications support at the early stages of design is critical to reducing time-to-market and minimizing costly redesigns for our customers.

Our product sales cycles can take up to 24 months to complete, requiring a significant investment in time, resources and engineering before realization of income from product sales, if at all. Such long sales cycles mean that OEM customers vendor selections, once made, are normally difficult to change. As a result, a design loss to the competition can negatively impact our financial results for several years. Similarly, design wins can result in an extended period of revenue opportunities with that customer.

We market and sell our products through our direct sales force and through approximately 17 independent sales representatives throughout the world. Our direct sales force is dedicated to enhancing relationships with our customers. We supplement our direct sales force with independent sales representatives, who have been selected based on their understanding of the networking systems market and their level of penetration at our target OEM customers. We also use application engineers to provide technical support and design assistance to existing and potential customers.

Our marketing group is responsible for market and competitive analyses and defining our product roadmaps and specifications to take advantage of market opportunities. This group works closely with our research and development group to align development programs and product launches with our OEM customers schedules. Additionally, this group develops and maintains marketing materials, training programs and our web site to convey our benefits to networking OEMs.

Research and Development

We devote substantial resources to the development of new products, improvement of existing products and support of the emerging requirements of networking OEMs. We have assembled a team of product designers

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possessing extensive experience in system architecture, analog and digital circuit design, hardware reference board design, software architecture and driver design and advanced fabrication process technologies. As of December 31, 2004, we had 55 full-time employees engaged in research and development. Our research and development expense was $17.3 million, $18.3 million and $17.1 million for the years ended December 31, 2004, 2003 and 2002, respectively.

We use a number of standard design tools in the design, manufacture and verification of our products. Due to the highly complex design requirements of our products, we typically supplement these standard tools with our own tools to create a proprietary design methodology that allows us to optimize the circuit-level performance of our products.

Technology

We have technological core competencies in the design of integrated circuits to enable network-aware processing using very large knowledge databases. Our products integrate in a single integrated circuit high performance processing, storage circuitry, control functionality and advanced I/O interfaces. Due to the highly specialized nature of our design process, we implement almost all portions of our product design without third party technology, with the exception of readily available intellectual property to implement standard functions, such as memory and timing control circuits.

We have assembled a research and development team with extensive expertise in the following areas:

Transistor-level Circuit Design. A common approach to application specific processor design is to use pre-defined logic functions. This approach is used extensively to shorten the development cycle by allowing an automated process for mapping a product s logical definition to its construction in silicon. In order to provide knowledge-based processors which feature high speed, low power dissipation and small form factors, we use a more fundamental approach using transistor-level circuit design. With this highly-customized design flow, we are able to implement processing elements that are defined at the most fundamental transistor level and therefore provide higher levels of performance. We employ standard simulation tools that are commonly used in the transistor-level design of analog products. We complement these tools with unique and proprietary methods to meet the complex design requirements of our knowledge-based processors.

Full-custom Layout. In order to implement a transistor-level circuit design, we use a full-custom layout flow to define how circuits are constructed in silicon. This flow enables us to control transistor characteristics to optimize circuit design and minimize chip size. By minimizing chip size, we are able to reduce the cost of our knowledge-based processors. This flow also enables us to control the precise layout of transistors and the connections between them in order to reduce power dissipation. Minimizing the power dissipated by integrated circuits becomes increasingly important for networking systems, which are increasingly designed in small form factors.

Advanced Design Architecture. By working closely with the engineering and design teams of our OEM customers, we utilize our design architecture skills to help ensure that our knowledge-based processors are deployed within their systems in a manner that best addresses their target applications. This product architecture task involves effective partitioning of our knowledge-based processors resources to multiple network decision processes, optimized timing to ensure efficient interfaces to other devices and determination of instruction sequences to allow for unique applications. We have acquired our advanced design architecture skills and application knowledge through close collaboration with networking OEMs during the development of successive generations of our products.

Device Physics. We possess a comprehensive understanding of device physics, which is important to the development of knowledge-based processors. This understanding includes not only the desired transistor characteristics to be implemented but also the way in which process variations can affect the operation of an

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integrated circuit. To mitigate these effects, we utilize our extensive knowledge of device physics and skills in conjunction with standard tools to make circuit-level design modifications or manufacturing process changes to improve the performance of our products.

Software Product Code and Development Tools. Our knowledge-based processors are delivered to our OEM customers with a suite of supporting software that is intended to accelerate the integration of our solution in their overall system environment. This product code includes knowledge database management software to assist in the initialization and management of records retained on our knowledge-based processors, as well as software used to communicate with our knowledge-based processor. In addition, we provide our OEM customers with emulation and modeling software for the design and verification of their software and hardware. We develop software packages using a team of engineers that possess advanced system knowledge and device modeling skills.

High-speed I/O Interface. Our products interface with high performance packet processors that utilize our knowledge-based processors to decide what action to take on an incoming packet of information. Due to the nature of this functional partitioning, a very high bandwidth connection is required between the packet processor and our knowledge-based processor. To meet the complex requirements of this interface, we develop custom high-speed I/O interfaces. We develop these circuits with advanced technology to support integrated circuit-to-integrated circuit communications.

Manufacturing

We design and develop our products and electronically transfer our proprietary designs to third party wafer foundries to manufacture our products. Wafers processed by these foundries are shipped to our subcontractors, where they are assembled into finished products and electronically tested before delivery to our customers. We believe that this manufacturing model significantly reduces our capital requirements and allows us to focus our resources on the design, development and marketing of our products.

Our principal wafer foundry is TSMC in Taiwan, and we also use UMC in Taiwan. We are actively involved with product development on next-generation processes, and are designing products on TSMC s 90-nanometer process geometries and higher. The latest generation of our products employs up to eight layers of copper interconnect and 300 millimeter wafer sizes.

Our products are designed to use industry standard packages and be tested using widely available automatic test equipment. We develop and control product test programs used by our subcontractors based on our product specifications. We currently rely on ASAT Holdings Limited in Hong Kong, Amkor Technology, Inc., Advanced Semiconductor Engineering, Inc. in Taiwan, King Yuan Electronics Co., Ltd. in Taiwan, ISE Labs, Inc. and Viko Test Lab in the U.S. to assemble and test our products. In February 2005, we established a representative office in Taiwan to employ local personnel to work directly with our Asian wafer manufacturers and assembly and test houses to facilitate manufacturing operations.

We have designed and implemented an ISO9001-certified quality management system that provides the framework for continual improvement of our products, processes and customer service. We apply well-established design rules and practices for CMOS devices through standard design, layout and test processes. We also rely on in-depth simulation studies, testing and practical application testing to validate and verify our products. We emphasize a strong supplier quality management practice in which our manufacturing suppliers are pre-qualified by our operations and quality teams. To ensure consistent product quality, reliability and yield, we closely monitor the production cycle by reviewing electrical, parametric and manufacturing process data from each of our wafer foundries and assembly subcontractors. We currently do not have long-term supply contracts with any of our significant third party manufacturing service providers. We generally place purchase orders with these providers according to terms and conditions of sale which specify price and 30-day payment terms and which limit the providers liability.

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Competition

The markets for our products are highly competitive. We believe that the principal bases of competition are:

- processing speed;
- power dissipation;
- size of the knowledge database that can be processed;
- price;
- product availability and reliability;
- customer support and responsiveness;
- timeliness of new product introductions; and
- credibility of supplier to design and manufacture product.

We believe that we compete favorably with respect to each of the bases identified above. However, some of our larger competitors have greater financial resources and a longer track record as a semiconductor supplier than we do. We anticipate that the market for our products will be subject to rapid technological change. As we enter new markets and pursue additional applications for our products, we expect to face competition from a larger number of competitors. Within our target market, we primarily compete with certain divisions of Cypress Semiconductor Corporation and Integrated Device Technology, Inc. or IDT. We expect to face competition in the future from our current competitors, other manufacturers and designers of semiconductors, and innovative start-up semiconductor design companies.

Intellectual Property

Our success and future growth will depend, in part, on our ability to protect our intellectual property. We rely primarily on patent, copyright, trademark and trade secret laws to protect our intellectual property. We also attempt to protect our trade secrets and other proprietary information through agreements with our customers, suppliers, employees and consultants and through security protection of our computer network and physical premises. However, these measures may not provide meaningful protection for our intellectual property.

As of December 31, 2004, we held 69 issued U.S. patents and 7 issued foreign patents. In addition, as of December 31, 2004, we had 73 patent applications pending in the U.S. We may not receive any additional patents as a result of these applications or future applications. Our U.S.

patents have expiration dates from 2017 through 2023. Nonetheless, we continue to pursue the filing of additional patent applications. Any rights granted under any of our existing or future patents may not provide meaningful protection or any commercial advantage to us.

While our patents and other intellectual property rights are important, we believe that our technical expertise and ability to introduce new products in a timely manner will also be important factors in maintaining our competitive position.

Many participants in the semiconductor industry have a significant number of patents and have frequently demonstrated a willingness to commence litigation based on allegations of patent and other intellectual property infringement. From time to time, we have received, and expect to continue to receive, notices of claims of infringement or misappropriation of other parties proprietary rights. We cannot assure you that we will prevail in these actions, or that other actions alleging infringement by us of third party intellectual property rights, misappropriation or misuse by us of third party trade secrets, or invalidity or unenforceability of our patents will not be asserted against us or that any assertions of infringement, misappropriation, misuse, invalidity or unenforceability will not materially and adversely affect our business, financial condition and results of operations.

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Equity Incentive Compensation explains the role of equity incentive awards in our compensation program

Compensation of Chief Executive Officer and *Compensation of Executive Chairman* summarizes the employment agreements that we have with our Chief Executive Officer and our Executive Chairman

Change in Control and Severance Arrangements explains the role of such arrangements in our compensation program

Elective Deferred Compensation Plan summarizes this plan and the role it has in our compensation program

Retirement Benefits Under the 401(k) Plan and Not-Generally-Available Benefit Program summarizes our retirement benefits under the 401(k) plan as well as other benefits provided to our executive officers that are not generally available to all of our employees

Medical and Dental Insurance Retirement Benefit summarizes this element of our compensation program

Executive Stock Ownership Guidelines sets forth the stock ownership guidelines that we have adopted for our executive officers

Accounting and Tax Considerations explain the accounting and tax matters that we consider when setting compensation

This CD&A discusses our executive compensation in the context of a calendar year because our compensation program is designed and evaluated on a calendar year basis rather than a fiscal year basis. However, as required by applicable SEC rules, the compensation tables that follow this CD&A report the executive compensation payments and awards made during fiscal year 2007.

Philosophy and Objectives

Lam Research's compensation program is designed and evaluated on a calendar year basis rather than a fiscal year basis because the Company's business planning, performance goal setting, pay and benefit cycles are all run on a calendar year. The principal objectives of our compensation program are to:

- Maintain competitive programs to attract, retain and motivate high-caliber executives,
- Maximize the Company's long-term success by appropriately rewarding executive officers for their achievements,
- Focus executive efforts on long-term strategic goals for the Company by closely aligning executive financial interests with stockholder interests while minimizing undue dilution of the Company's shares, and
- Structure compensation programs to take into account the accounting treatment and tax deductibility of executive compensation expense.

In formulating and administering the individual elements of our executive compensation program we focus on:

- Developing compensation packages for our executive officers that are comparable to similarly situated executives in high technology companies;
- Emphasizing pay for performance that rewards achievement of both short- and long-term business objectives;
- Establishing appropriate quantitative and strategic performance objectives and metrics; and
- Matching recognition of compensation expense as much as possible to the fiscal period in which performance occurs.

Within this framework, the Committee reviews the information, analysis and compensation proposals provided by management and meets with our Executive Chairman, senior management, and specialists from Human Resources, Finance and Legal. Management makes recommendations to the Committee on the base salary, annual incentive award targets and long-term incentive compensation for the named executive officers. The Committee considers management's recommendations with respect to executive compensation in light of competitive compensation data and relevant business objectives. At the request of the Committee, the Executive Chairman discusses management's compensation recommendations with the Committee. The Committee also regularly holds executive sessions not attended by any members of management. The Committee makes recommendations to the independent members of our Board of Directors on the compensation of our Chief Executive Officer for the final determination and approval by such members of our Board of Directors.

Executive Compensation Program Components and Process

Components. Lam Research's executive compensation program consists of the major components listed in the table below. We consider each element to be appropriate to meet one or more of the principal objectives of our compensation policy. We generally target compensation near the 50th percentile of our peer group, yet allow our executives the ability to achieve higher levels of compensation (up to and above the 75th percentile of our peer group) if warranted by superior company and individual performance. Furthermore, we also consider factors such as job performance, job scope and responsibilities, skill set, prior experience, the executive's time in his or her position with Lam Research, internal consistency regarding pay levels for similar positions or skill levels within the Company, external pressures to attract and retain talent, and market conditions generally. In general, pay differentials between our executive officers reflect these factors and we believe are consistent with pay differentials between similar positions at our peer companies.

Component	Purpose	Target Market Position
1. Base salary	Enable recruitment and retention of high caliber employees at a competitive level of compensation	50th percentile
2. Annual incentive awards	Reward executives for achieving shorter-term corporate and functional performance objectives	50th – 75th percentile, depending on performance results
3. MYIP	Align executive performance goals with corporate objectives associated with long-term shareholder value creation; promote executive retention	50th – 75th percentile, depending on performance results
4. Deferred compensation benefits		
5. Retirement benefits	Provide competitive benefits; promote executive retention	50th percentile
6. Other benefit programs		

We also have included severance provisions in employment agreements we have entered into with Messrs. Bagley, Newberry and Bright. These employment agreements are described in more detail below as well as in the "Potential Payments Upon Termination or Change-in-Control" section below. We typically do not offer severance provisions in our agreements with executive officers but we retain the flexibility to do so on an individual basis for recruitment and retention purposes and in order to provide a period during which a former executive is incentivized not to engage in competitive activities.

Process: Generally. At the beginning of each calendar year, the Committee reviews base salaries, annual incentives and long-term incentives and revises the overall compensation package from time to time when appropriate in light of Lam Research's current business strategies and performance and changes in regulatory, tax and accounting rules and interpretations, while also taking into account the interests of our stockholders. For instance, in 2006, we substantially revised the long-term incentive element of our compensation program when we introduced the Multi-Year Cash-Based Incentive Program ("MYIP") in consideration of, among other concerns,

changes to accounting rules regarding expense recognition for equity-based awards.

When appropriate, the Committee has also adjusted compensation components to account for the level of previous earnings by an executive officer. For example, in February 2006, the Committee provided a supplemental one-year plan under the MYIP for Messrs. Anstice, Maddock and Hariri in consideration for the absence of equity incentive grants to them in the years prior to the adoption of the MYIP and the relatively low level of equity incentive awards made to them in comparison to executive officers in similar positions from our peer group. Messrs. Anstice, Maddock, and Hariri have not received an equity award since 2002.

Process: Annual Incentive Awards. Our annual incentive awards provide for cash payments based on the corporate, organizational and individual performance results achieved each calendar year. Corporate performance is determined primarily by operating income as a percent of revenue. Organizational and individual performance metrics generally fall in one or more of the following categories: business process improvement, customer relationships, market share gains, organizational capability, new product development, decreased cycle times, and employee retention efforts. Typically, the Committee meets in January and/or February to review the operating profit performance target and target incentive amounts for the first half of the calendar year and in August to review those targets for the second half of the calendar year. By reviewing performance targets and incentive amounts every six months, the Committee retains the ability to make adjustments as necessary to reflect changing business conditions and corporate objectives.

Process: MYIP. The MYIP was designed and proposed to the Committee by management and is a program under Lam Research's stockholder-approved 2004 Executive Incentive Plan (the "EIP"). The cash-based incentive structure of the MYIP is intended to provide competitive levels of compensation to our senior executives while (i) allowing the Company to accrue compensation expense during the period in which performance occurs, (ii) as a non-equity program, minimizing dilution of stockholder value, and (iii) incentivizing senior management retention by generally requiring continuous employment through the payment determination date which is typically approximately two years following the start of the performance period. Performance factors are established by the Committee annually and funding is accrued on a periodic basis. A new MYIP cycle typically commences at the beginning of each calendar year and lasts for eight consecutive calendar quarters. For instance, our first MYIP cycle commenced in the first quarter of calendar year 2006 and ran through the end of calendar year 2007 (the "2006 MYIP"), a second MYIP commenced in the first quarter of calendar year 2007 and runs through the end of calendar year 2008 (the "2007 MYIP"), and a third MYIP commenced in the first quarter of calendar year 2008 and runs through the end of calendar year 2009 (the "2008 MYIP"). To date, the MYIP performance metrics have been comprised of a formula based on attainment of the Company's operating profit target for each year and stock price, because the Committee believes these measurements represent the best indicators of the performance of the Company and our executive team during the performance periods. For the 2006 MYIP, target award levels were determined after consideration of a study conducted during 2005 and 2006 by Mercer Consulting, an objective third party consulting firm. Mercer Consulting was engaged by management to provide information on the amounts that executives of the peer group realized pursuant to long-term equity-based incentive programs and to provide a recommendation on a competitive target award in lieu of equity grants for participants of the 2006 MYIP. For the 2007 and 2008 MYIPs, the Committee (and the independent members of the Board with respect to the CEO) set target awards after consideration of the overall compensation package for the named executive officers, the potential rewards from the MYIP and the competitive compensation environment. Typically, the Committee (and the independent members of the Board with respect to the CEO) meets in January and/or February to review and determine the operating profit performance metric for the then-current calendar year for each cycle of the MYIP then in effect.

Process: Setting Targets. The Committee establishes performance goals so that the specific performance targets will be challenging but achievable based on expected levels of performance from executive officers while providing that below expected performance would reduce the executive's award. Performance goals are set such that very strong performance is required to earn payments above the target bonus amounts. The Company believes that our specific operating profit targets for awards granted as annual incentive awards and under the MYIP are confidential information and their disclosure would result in competitive harm to the Company. In 2006 and 2007 Lam Research achieved significant market share growth, leading to a substantial expansion of revenues and profitability growth. Together, these results led to the payment of above target bonuses as annual incentive awards and contributed to a maximum payout under the applicable MYIP performance cycle. For calendar years 2007 and 2008, the Committee revised the operating profit growth targets upward to provide a greater degree of difficulty in meeting those targets in light of the business plan and outlook each year.

Peer Group

The Committee also determines the levels of compensation and the mix and weighting of compensation components after reviewing data from a peer group of comparably-sized companies in the high technology industry and from nationally published survey data.

The peer group companies are selected based on their comparability to Lam Research's revenue size and business purpose, and with whom we believe we are likely to compete for talent. Based on these criteria, the peer group may be modified from one year to the next. For calendar year 2007, the peer group consisted of the following companies:

Analog Devices, Inc.
Applied Materials, Inc.
Cymer, Inc.
Cypress Semiconductor Corporation
Fairchild Semiconductor International, Inc.
KLA-Tencor Corporation
LSI Corporation
MEMC Electronic Materials, Inc.
Molex Incorporated
National Semiconductor Corporation
Novellus Systems Inc.
NVIDIA Corporation
Plexus Corp.
SanDisk Corporation
Teradyne, Inc.
Varian Semiconductor Equipment Associates, Inc.
Xilinx, Inc.

In addition to peer group data, our human resources department engaged outside consultants from Radford, the Presidio Group and F.W. Cook & Co. to analyze published survey market data on base salary, bonus targets, equity awards and total compensation.

Base Salary

For 2007 and 2008, after taking into consideration peer group compensation and management's recommendations, the Committee (and the independent members of the Board with respect to the CEO) set the base salaries of each of the named executive officers (see table below) as follows:

Name	Calendar Year 2006	Calendar Year 2007	Calendar Year 2008
Stephen G. Newberry	$710,000	$800,000	$800,000
Martin B. Anstice	$340,000	$380,000	$400,000
Ernest E. Maddock	$375,000	$400,000	$416,000
Abdi Hariri	$275,000	$300,000	$315,000
Richard A. Gottscho	$312,000	$340,000	$360,000
Nicolas J. Bright	$435,000	$461,100*	NA*

* In connection with Mr. Bright's Employment Agreement, his base salary was further increased to $500,000 in February 2007. The Company does not expect Mr. Bright to be a named executive officer for fiscal year 2008.

Annual Incentive Awards

Generally

Annual incentive awards for our executive officers for a specific calendar year are based on an individual performance factor, a corporate performance factor and a target bonus amount based upon a percentage of annual eligible salary. The actual incentive award is calculated by multiplying the individual factor by the corporate factor by the target bonus amount. The portion of the award based upon individual performance is subject to a maximum multiplier determined at the beginning of the calendar year. The corporate performance

factor is applied using a fixed ratio based on the Company's actual operating profit achievement. The calculated incentive award for executive officers (other than the CEO) may be increased by the Committee, and may be subject to negative discretion by the Committee (or the independent members of the Board with respect to the CEO) after the performance period.

The individual metrics for calendar years 2006 and 2007 were given equal weight with the corporate performance factor which was based upon operating income as a percent of revenue. These objectives and relative weightings were selected based upon management recommendations and Committee and Board determination that they represented the most important metrics of company performance during the applicable calendar years and as a complement to the focus on the operating profit metric under the MYIP discussed below. For calendar years 2006 and 2007, the portion of the award based upon individual performance was subject to a maximum multiplier of 1.5 on the performance factor.

Mr. Newberry

Annual incentive awards for Mr. Newberry for calendar years 2006, 2007, and 2008 were made under Lam Research's EIP so that his bonus amounts would qualify for deductibility under Section 162(m) of the Internal Revenue Code of 1986, as amended ("Section 162(m)"), discussed further below.

Calendar Year 2006. The Board approved Mr. Newberry's target bonus amount for calendar year 2006 at 100% of his annual eligible salary. The metrics for Mr. Newberry's individual performance were market share (weighted at 30%), revenue and gross margin (weighted at 35%) and cash from operations (weighted at 35%). These objectives, together, were given equal weight with the corporate performance factor which was based upon operating income as a percent of revenue. For calendar year 2006, no discretion was exercised by the Board in determining Mr. Newberry's annual incentive award. Mr. Newberry's actual calendar year 2006 incentive award was calculated at 2.13 times his target bonus amount, equal to a payout of $1,485,716. This amount is included in the Non-Equity Incentive Plan Compensation column of the Summary Compensation Table below.

Calendar Year 2007. In February 2007, the Committee selected, and the independent members of the Board approved, the annual bonus plan factors for Mr. Newberry for calendar year 2007 and established targets for the first half of calendar 2007. Each of the factors and their relative weighting for Mr. Newberry's 2007 annual bonus award were unchanged from the 2006 calendar year plan except that under the corporate performance factor, actual operating profit growth targets were revised upward to provide a greater degree of difficulty in meeting those targets in light of the business plan and outlook for calendar year 2007. No changes were made to Mr. Newberry's performance targets for the second half of calendar year 2007. For calendar year 2007, no discretion was exercised by the Board in determining Mr. Newberry's annual incentive award. In February 2008, the Committee recommended and the independent members of the Board approved that Mr. Newberry's calendar year 2007 annual incentive award be calculated at 1.80 times his target bonus amount, equal to a payout of $1,427,690.

Calendar Year 2008. In March 2008, based upon the Committee's recommendations, the independent members of the Board approved Mr. Newberry's target bonus amount for calendar year 2008 at 125% of base salary, subject to a cap of 2.25 times the target bonus amount.

Other Named Executive Officers

The individual performance factors for each executive also include organizational performance objectives based upon applicable business unit performance goals. These objectives generally fall in one or more of the following categories: business process improvement, customer relationships, market share gains, organizational capability, new product development, decreased cycle times, and employee retention efforts. Target bonus amounts ranged from 65% to 85% of annual salary for each executive. The differences in target bonus amounts among the named executive officers are determined based on job scope and responsibilities and the competitive compensation data.

Calendar Year 2006. In February 2007, the Committee approved incentive award payouts for calendar year 2006 performance at amounts ranging from 1.90 to 2.05 times the executives target bonus award reflecting each executives individual performance results. Actual dollar amounts are reported in the Non-Equity Incentive Plan Compensation column of the Summary Compensation Table below. The Committee did not exercise discretion to increase or reduce any awards during calendar year 2006.

Calendar Year 2007. In January 2008, the Committee approved incentive award payouts for calendar year 2007 performance at amounts ranging from 1.61 to 1.80 times the executives target bonus award reflecting each executives individual performance results against the organizational objectives mentioned above.

Calendar Year 2008. In January 2008, new target bonus amounts for calendar year 2008 were set for the other named executive officers. These amounts range from 70% to 80% of annual salary for each executive, subject to a cap of 2.25 times the target bonus amount.

Earned annual incentive awards for calendar years 2005, 2006, and 2007 are provided in the table below for the named executive officers.

	Earned Annual Incentive Award		
	Calendar Year	Calendar Year	Calendar Year
Name	**2005**	**2006**	**2007**
Stephen G. Newberry	$944,568	$1,485,716	$ 1,427,690
Martin B. Anstice	$350,437	$ 447,212	$ 503,258
Ernest E. Maddock	$362,135	$ 510,745	$ 490,602
Abdi Hariri	$220,600	$ 328,354	$ 332,268
Richard A. Gottscho	$274,938	$ 419,207	$ 403,546
Nicolas J. Bright	$494,236	$ 744,543	NA*

* The Company does not expect Mr. Bright to be a named executive officer for fiscal year 2008.

Multi-Year Cash-Based Incentive Program (MYIP)

The Committee selects certain executives to participate in each MYIP. During 2006 and 2007, cash awards under the MYIP were the only long-term incentive awards provided for the named executive officers with the exception of Mr. Gottscho, who received a grant of restricted share units but was not a participant in the 2006 or 2007 MYIPs. In addition, Messrs. Anstice, Maddock, and Hariri participated in a supplemental one-year plan under the MYIP based on the Companys operating profit performance which covered performance in calendar year 2006. Awards under the supplemental plan were determined and paid in February 2007. The Committee established this supplemental plan in consideration of the absence of equity incentive grants to the participants since calendar year 2002.

In order to receive an award under the MYIP, participants generally must be continuously employed at Lam Research through the date(s) on which the Committee determines the actual award amounts under the applicable program (the determination date). The Committee has the discretion to waive or otherwise adjust the retention criteria for individual participants. For example, Mr. Bright is eligible to receive the target incentive amount established for his 2007 calendar year performance under the 2007 MYIP, since Mr. Bright remained employed by Lam Research through a vesting date of March 1, 2008.

The Companys named executive officers excluding Mr. Gottscho were eligible for performance-based awards under the following MYIPs:

MYIP	Performance Period	Determination Date	Eligible NEOs
Supplemental	Jan. 2006 Dec. 2006	February 2007	Messrs. Anstice, Maddock & Hariri
2006	Jan. 2006 Dec. 2007	February 2008	All (excluding Gottscho)

2007	Jan. 2007 – Dec. 2008	February 2009*	All (excluding Gottscho)
2008	Jan. 2008 – Dec. 2009	February 2010	All**

* March 1, 2008 for Mr. Bright.

** Mr. Bright is not a participant of the 2008 MYIP.

MYIP Performance Periods

Performance factors, comprised of a formula based on the attainment of the Company's operating profit target, are established by the Committee annually and measured and accrued on a quarterly basis. In February 2006, the Committee (and the independent members of the Board with respect to the CEO) established the operating profit performance metric upon which actual incentive awards would be calculated for calendar 2006. In January 2007, the Committee (and the independent members of the Board with respect to the CEO) established the operating profit performance metric upon which actual incentive awards would be calculated for calendar 2007 under both the 2006 and 2007 MYIPs. In January 2008, the Committee established the operating profit performance metric upon which actual incentive awards would be calculated for calendar year 2008 under both the 2007 and 2008 MYIPs for the Company's named executive officers excluding Mr. Newberry. In March 2008, based on recommendations of the Committee, the independent members of the Board established this metric for Mr. Newberry.

Additionally, the 2006, the 2007, and the 2008 MYIPs provide that the calculated award amounts are automatically increased (but may not be decreased) pursuant to a ratio comparing the Company's stock price performance over the 50 trading day trailing average as of the end of each fiscal quarter to the 200 trading day trailing average as of the beginning of the respective program. Under each program, the actual award payable to each participant cannot exceed 2.5 times the target bonus amount set for each plan. During calendar year 2006 and 2007, the stock price factor did positively affect the amounts calculated pursuant to the formula set forth in the respective MYIP.

The Committee (and the independent members of the Board with respect to the CEO) has the opportunity to review the provisional accruals on a periodic basis and may choose to exercise negative discretion to reduce the amount of award accruals following such review. The Committee (and the independent members of the Board with respect to the CEO) did not exercise its negative discretion to reduce any award accruals during calendar years 2006 or 2007, with the exception of Mr. Bright, whose 2006 MYIP award payment was reduced from the calculated amount.

The aggregate individual target award amounts and the aggregate amounts earned for the named executive officers under each cycle of the MYIP (except for Mr. Gottscho who participates in the 2008 MYIP only) were:

MYIP	Aggregated Individual Target Amounts	Aggregated Individual Earned Awards	Earned Award as a % of Target Amount
2006	$8,325,000	$20,567,500	247%
2007	$9,157,500	NA(1)	NA(1)
2008(2)	$9,214,500	NA(3)	NA(3)
Supplemental	$2,520,000	$ 3,872,300	154%

(1) Earned awards under the 2007 MYIP are scheduled for a February 2009 payment.

(2) Mr. Bright is not a participant of the 2008 MYIP.

(3) Earned awards under the 2008 MYIP are scheduled for a February 2010 payment.

Equity Incentive Compensation

The Company believes that long-term equity incentive awards can be a useful part of its executive compensation program. However, as discussed above, the Company has chosen to grant primarily long-term cash incentive awards to its executive officers for calendar years 2006 and 2007. The Committee or Board may use its discretion to grant stock options or restricted stock units to executive officers in the future to provide competitive long-term incentives and to reward behaviors that result in long-term stockholder value growth. At this time, the Company does not have a formal policy with respect to the timing of granting equity awards.

Compensation of Chief Executive Officer

The Company and Mr. Newberry entered into an employment agreement (the "Newberry Agreement") effective January 1, 2003, which continues in effect pursuant to an automatic one-year renewal provision. The Newberry Agreement provides for a base salary at a rate to be set at least annually by the Board. Under the Newberry Agreement, Mr. Newberry is entitled to participate in any performance incentive plan offered by the Company, in the Company's executive deferred compensation plan(s), and in other benefit and compensation programs generally applicable to key executives of the Company. The Newberry Agreement includes severance provisions which are described below in the "Potential Payments Under Termination of Employment or Change-in-Control" section below.

Compensation of Executive Chairman

The Company and Mr. Bagley entered into a new employment agreement (the "Bagley Agreement") effective January 1, 2006. The term of the Bagley Agreement is from January 1, 2006, to March 31, 2009, unless extended or earlier terminated in accordance with its provisions. Pursuant to the terms and conditions of the Bagley Agreement, Mr. Bagley will continue to serve as Executive Chairman of the Company during the term of the agreement. Mr. Bagley will receive an annual salary of $240,000 provided he remains employed by the Company. Subject to certain non-compete and other terms and conditions, the Bagley Agreement provides for a lump sum payment of $2.5 million on April 15, 2009. During the term of the Bagley Agreement, Mr. Bagley will not participate in any executive bonus plans maintained by the Company. Mr. Bagley however is eligible to participate in the standard executive benefit plans maintained by the Company. During the term of the Bagley Agreement, Mr. Bagley agrees not to perform services for any other for-profit enterprise that would interfere with his services to, or otherwise compete with, the Company. The Bagley Agreement includes severance provisions which are described below in the "Potential Payments Upon Termination or Change-in-Control" section below.

Change in Control and Severance Arrangements

Lam Research generally does not provide for severance or change in control benefits to executive officers except for individually negotiated arrangements such as those with Messrs. Newberry, Bagley and Bright. These arrangements are more fully described in the "Potential Payments Upon Termination of Employment or Change-in-Control" section below. We use such individually negotiated arrangements for recruitment and retention purposes and in order to provide a period during which a former executive will be incentivized not to engage in competitive activities.

However, as discussed below, we do provide medical and dental insurance retirement benefits to eligible former officers (and members of our Board). Furthermore, certain of the Company's stock option plans and its Employee Stock Purchase Plan provide that, upon a merger of the Company with or into another corporation or the sale of substantially all of the assets of the Company, some or all of the options granted under certain of the stock option plans shall be accelerated so as to be fully exercisable, and all of the rights granted under the Employee Stock Purchase Plans shall be fully exercisable following the merger for a period from the date of notice by the Board. Following the expiration of such periods, the options and rights will terminate. The 2007 Stock Incentive Plan adopted by Company stockholders at the 2006 Annual Meeting allows the Company broad discretion to provide for vesting acceleration of awards on change-of-control transactions.

Elective Deferred Compensation Plan

Lam Research maintains a non-qualified deferred compensation plan, the Elective Deferred Compensation Plan (the "EDCP"), which allows eligible employees, including executive officers, to voluntarily defer receipt of all or a portion of his/her salary and all or a portion of a bonus payment until the date or dates elected by the participant, thereby allowing the participating employee to defer taxation on such amounts. The EDCP is offered to eligible employees, including the named executive officers, in order to allow them to defer more compensation than they would otherwise be permitted to defer under a tax-qualified retirement plan, such as The Lam Research Corporation Employee Savings Plus Plan (the "401(k) Plan"). Further, Lam Research offers the EDCP as a competitive practice to enable it to attract and retain top talent.

The EDCP is evaluated by the human resources group for competitiveness in the marketplace from time to time, but the level of benefits provided is not typically taken into account in determining an executive's overall compensation package for a particular year due to its conservative nature.

Retirement Benefits Under the 401(k) Plan and Not-Generally-Available Benefit Programs

Each of Lam Research's named executive officers is eligible for additional benefits generally available to Company employees such as matching contributions to Lam Research's 401(k) plan and medical coverage benefits. Lam Research also provides additional benefits to its named executive officers that are not generally available to other Company employees, including the payment of term life insurance premiums, payment of medical co-insurance premiums and matching contributions to the EDCP in lieu of decreased contributions that would otherwise have been made had such EDCP deferrals not been made. The amount of the Company EDCP contribution that is not generally available to other Company employees is shown in the "All Other Compensation Table" below.

Medical and Dental Insurance Retirement Benefit

The Company provides a program to pay for post-retirement medical and dental insurance coverage for eligible former executive officers and members of Lam's Board of Directors. To be eligible, a person must have served at the position of vice president or above or as a member of the Board of Directors, be at least age 55 at retirement, and have at least five years of continuous service with Lam Research. An executive officer or director must be enrolled in the Company's U.S. group medical and dental plans at the time of his or her retirement. When the retired person reaches age 65, he or she is required to enroll in Medicare parts A and B which would be the primary payer for the executive's health coverage. The benefit also covers the person's spouse at the time of retirement for his or her lifetime as well as other eligible dependents. The benefit ceases if the person becomes employed by a competitor of Lam Research after leaving the Company's service. We provide the benefit to our executives and members of our board to further the long-term retention of their services and/or provide a disincentive to later compete against the Company.

Executive Stock Ownership Guidelines

During fiscal year 2006, the Company adopted executive stock ownership guidelines, pursuant to which senior executives are expected and encouraged to own and maintain certain minimum levels of the Company's Common Stock. The Committee believes that these guidelines are an appropriate addition to the Company's equity compensation policies and, in conjunction with Lam Research's equity and cash-based incentive plans, will further serve to align the long-term interests of the senior executives with those of the Company's stockholders. Each executive is required to accumulate and maintain ownership of shares of the Company's Common Stock, in the quantities indicated by the guidelines below, by the later of December 31, 2010, or the fifth anniversary of an executive's hire date.

Position	Stock Ownership Guideline
Chief Executive Officer	5X Salary
Chief Financial Officer	3X Salary

All other senior executives	2X - 3X Salary

Accounting and Tax Considerations

Section 162(m). In determining which elements of compensation are to be paid, and how they are weighted, Lam Research also takes into account whether a particular form of compensation will be considered performance-based compensation for purposes of Section 162(m) of the Internal Revenue Code. Under Section 162(m), Lam Research generally receives a federal income tax deduction for compensation paid to any of its named executive officers only if the compensation is less than $1 million during any fiscal year or is performance-based under Section 162(m). In 2004, Lam Research adopted the EIP with a structure intended to provide for the tax deductibility of awards granted under the EIP. Accordingly, during fiscal 2007, the annual incentive awards granted to Mr. Newberry and to the greatest extent possible, all MYIP grants to Mr. Newberry and the other named executive officers were granted under Lam Research s EIP. In November 2006, our stockholders approved an amendment to the EIP that increased the amount of cash awards that may be paid to any one participant in respect of achievement of performance goals for any twelve-month period to $12 million. Prior to the amendment, the maximum amount of awards that could be paid to a participant in a twelve-month period and qualify for deductibility under Section 162(m) was $2 million. Accordingly, we expect that all MYIP grants made after passage of the amendment will qualify for deductibility under Section 162(m). The prior $2 million limit for deductibility will likely apply to performance periods under grants prior to the amendment. The Committee currently intends to continue to seek a tax deduction for all of Lam Research s executive compensation, to the extent it determines it is in the best interests of Lam Research.

Section 409A. To assist in the avoidance of additional tax under Section 409A of the Internal Revenue Code, Lam structured the MYIP and the EDCP, and structures its equity awards, in a manner intended to comply with the applicable Section 409A requirements.

As a result of the Company s voluntary review of its historical stock option granting process and conclusions reached by the Company, on March 30, 2008, the Board authorized the Company (i) to satisfy the potential Section 409A liability to current and past employees (including the named executive officers) arising as a result of their exercise of misdated stock options, which vested after December 31, 2004, in 2006 or 2007 (misdated options) and, as applicable, similar state tax laws, inclusive of applicable penalties and interest (collectively, the 409A Liability), and (ii) if necessary, to compensate such employees (including the named executive officers) for the additional tax liability associated with the Company s assumption of the 409A Liability (gross-up payment). The estimated 409A Liability is calculated on the entire amount of income recognized by the executive as a result of the exercise of the misdated options.

The table below lists the amount of estimated 409A Liability, including gross-up payments, that will be paid to or on behalf of the listed named executive officers.

Name	Estimated Cash 409A Liability, including gross-up $ million
Stephen G. Newberry	$10.3
Richard A. Gottscho	$ 0.5
Abdi Hariri	$ 0.2

For more information regarding the Company s voluntary review into its historical stock option granting process, please read the Company s Form 10-K for the year ended June 24, 2007, filed on March 31, 2008. For more information regarding the 409A Liability, please read the Company s Form 8-K filed on April 2, 2008.

Other Tax Considerations. It is Lam s general philosophy not to provide any executive officer or director with a gross-up or other reimbursement for tax amounts the individual might pay pursuant to Section 280G of the Internal Revenue Code.

Mr. Hariri received taxable income in fiscal year 2007 on the tax payments made on Mr. Hariri's behalf by the Company to compensate for the difference in income tax liabilities resulting from an expatriate assignment.

Summary Compensation Table

Name and Principal Position	Fiscal Year	Salary	Bonus	Stock Awards (3)	Option Awards (4)	Non-Equity Incentive Plan Compensation	Change in Pension Value and Nonqualified Deferred Compensation Earnings (11)	All Other Compensation (12)
Stephen G. Newberry Chief Executive Officer and President	2007	$759,039	$	$	$3,013	$7,588,859(5)	$808	$19,602
Martin B. Anstice Senior Vice President, Chief Financial Officer	2007	353,077			479	4,189,847(6)		26,397
Ernest E. Maddock Senior Vice President, Global Operations	2007	383,174			2,681	3,369,508(7)	3	21,429
Abdi Hariri Group Vice President, Customer Support Business Group	2007	283,173			1,028	2,728,276(8)	66	26,987
Richard A. Gottscho Group Vice President and General Manager, Etch Businesses	2007	327,692		747,356	1,194	419,207(9)	729	24,621
Nicolas J. Bright(1) Executive Vice President of Products	2007	456,250	787,500(2)		7,712	1,925,690(10)	633	26,463

Salary, bonus, and non-equity incentive plan compensation above includes amounts earned in fiscal year 2007 even if deferred at the election of the executive officer under the Company's deferred compensation plans and/or the Company's 401(k) Plan. All amounts listed as "Executive Contributions" in the "Non-Qualified Deferred Compensation Table" below represent contributions on amounts earned during fiscal year 2007 and disclosed in the Summary Compensation Table above.

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(1) Mr. Bright was the Company's Executive Vice President, Regional Business & Global Products until his transition to his present, non-Section 16 officer position on March 1, 2007.

(2) In March 2007, in connection with Mr. Bright's transition to his current position with Lam Research, the Committee approved, and the Company and Mr. Bright entered into; an arrangement whereby Mr. Bright will at minimum receive the target incentive amount established for his 2007 calendar year performance under the Company's 2007 MYIP provided that Mr. Bright remained employed by Lam Research through a vesting date of March 1, 2008. The $787,500 above represents the amount attributable to fiscal year 2007 under this arrangement.

(3) Amounts shown do not reflect compensation actually received by the named executive officer. Instead, the amounts shown are the compensation expenses recognized by Lam Research in fiscal 2007 for restricted stock units as determined pursuant to FASB Statement of Financial Accounting Standards Number 123(revised) Share-Based Payment (SFAS 123R). These compensation expenses reflect restricted stock units granted during fiscal 2007 and prior to fiscal 2007.

(4) Amounts shown do not reflect compensation actually received by the named executive officer. Instead, the amounts shown are the compensation expenses recognized by Lam Research in fiscal 2007 for option awards as determined pursuant to SFAS 123R. These compensation expenses reflect option awards granted prior to fiscal 2007. These compensation expenses reflect option awards granted during fiscal year 2002. The assumptions used to calculate the fair value of these option awards are set forth in Note M in Notes to Consolidated Financial Statements of the Company s Annual Report on Form 10-K for the fiscal year ended June 30, 2002.

(5) Represents $1,485,716 earned by Mr. Newberry pursuant to his 2006 annual incentive award (which was made under the EIP and pursuant to the Company's annual bonus plan for calendar year 2006), $4,718,128 accrued on Mr. Newberry's behalf for performance during fiscal 2007 under the 2006 MYIP and $1,385,015 accrued for performance during